

10 transactions between the multiprocessor modules (QPi), the second interconnection  
 11 level (SI) comprising external connection nodes (NCEj) connecting the nodes (Nj) to  
 12 one another and handling the transactions between the nodes (Nj), the connection  
 13 agents (NCSi) and the external connection nodes (NCEj) respectively having the same  
 14 basic structure, the same external interface (XI), and adapted to implement the same  
 15 coherency control protocol for the cache memories of the processors.

1 14. A modular interconnection architecture according to claim 13,  
 2 characterized in that each external connection node (NCEj) comprises two identical  
 3 connection agents (NCSi) connected head-to-tail, one of the two agents (NCS'j)  
 4 receiving and filtering transactions sent by the node (Nj) to which it is connected, and  
 5 the other agent (NCS''j) receiving and filtering the transactions sent by the other nodes  
 6 (Nj) to which it is connected.

1 15. A modular interconnection architecture according to claim 13,  
 2 characterized in that each connection agent (NCSi) comprises an associative memory  
 3 (DDi) with a fixed size determined as a function of the number of processors in the  
 4 multiprocessor module (QPi) to which the connection agent (NCSi) is connected, the  
 5 state of the memories (DDi) being indicative of the presence of the last modified data  
 6 blocks in the cache memories of the multiprocessor module (QPi).

1 16. A modular interconnection architecture according to claim 14,  
 2 characterized in that each connection agent (NCSi) comprises an associative memory  
 3 (DDi) with a fixed size determined as a function of the number of processors in the  
 4 multiprocessor module (QPi) to which the connection agent (NCSi) is connected, the  
 5 state of the memories (DDi) being indicative of the presence of the last modified data  
 6 blocks in the cache memories of the multiprocessor module (QPi).

1 17. A modular interconnection architecture according to claim 14,  
 2 characterized in that the first and second head-to-tail connection agents (NCS'j and  
 3 NCS''j) only accept transactions for blocks modified in their respective associative  
 4 memories (DD'j and DD''j); modified data blocks in the first connection agent (NCS'j)  
 5 being exported to the requesting multiprocessor module or modules and, conversely,

6 modified data blocks in the second connection agent (NCS"j) being imported from the  
7 module or modules holding the blocks.

1 18. A modular interconnection architecture according to claim 13,  
2 characterized in that the second interconnection level (SI) has a latency that is double  
3 the latency of the first interconnection level (MI).

1 19. A modular interconnection architecture according to claim 14,  
2 characterized in that the second interconnection level (SI) has a latency that is double  
3 the latency of the first interconnection level (MI).

1 20. A modular interconnection architecture according to claim 15,  
2 characterized in that the second interconnection level (SI) has a latency that is double  
3 the latency of the first interconnection level (MI).

1 21. A modular interconnection architecture according to claim 16,  
2 characterized in that the second interconnection level (SI) has a latency that is double  
3 the latency of the first interconnection level (MI).

1 22. A modular interconnection architecture according to claim 17,  
2 characterized in that the second interconnection level (SI) has a latency that is double  
3 the latency of the first interconnection level (MI).

1 23. A process for expanding the capacity of a machine comprising a first  
2 given number of processors on a first level (MI) organized into a first given number  
3 of multiprocessor modules (QPi) and capable of being inserted into an interconnection  
4 architecture comprising a modular interconnection architecture for an expandable  
5 multiprocessor machine, based on a virtual bus hierarchy, comprising a given number  
6 of multiprocessor modules (QPi), each comprising a plurality of processors and  
7 associated cache memories organized into nodes (Nj) and distributed on at least two  
8 interconnection levels: a first interconnection level (MI) corresponding to  
9 interconnection of the multiprocessor modules (QPi) within a node (Nj), and a second  
10 interconnection level (SI) corresponding to the interconnection of the nodes (Nj) with

11 one another, the first interconnection level (MI) comprising connection agents (NCSi)  
 12 connecting the multiprocessor modules (QPi) to one another and handling the  
 13 transactions between the multiprocessor modules (QPi), the second interconnection  
 14 level (SI) comprising external connection nodes (NCEj) connecting the nodes (Nj) to  
 15 one another and handling the transactions between the nodes (Nj), the connection  
 16 agents (NCSi) and the external connection nodes (NCEj) respectively having the same  
 17 basic structure, the same external interface (XI), and adapted to implement the same  
 18 coherency control protocol for the cache memories of the processors, characterized in  
 19 that it consists of disconnecting one of the first-level multiprocessor modules (QPi)  
 20 from its connection agent (NCSi) to free said connecting agent and of connecting, via  
 21 said freed connection agent, a second given number of processors organized into a  
 22 second given number of multiprocessor modules, also capable of being inserted into  
 23 said interconnection architecture.

1 24. A process for expanding the capacity of a machine comprising a first  
 2 given number of processors on a first level (MI) organized into a first given number  
 3 of multiprocessor modules (QPi) and capable of being inserted into an interconnection  
 4 architecture comprising a modular interconnection architecture for an expandable  
 5 multiprocessor machine, based on a virtual bus hierarchy, comprising a given number  
 6 of multiprocessor modules (QPi), each comprising a plurality of processors and  
 7 associated cache memories organized into nodes (Nj) and distributed on at least two  
 8 interconnection levels: a first interconnection level (MI) corresponding to  
 9 interconnection of the multiprocessor modules (QPi) within a node (Nj), and a second  
 10 interconnection level (SI) corresponding to the interconnection of the nodes (Nj) with  
 11 one another, the first interconnection level (MI) comprising connection agents (NCSi)  
 12 connecting the multiprocessor modules (QPi) to one another and handling the  
 13 transactions between the multiprocessor modules (QPi), the second interconnection  
 14 level (SI) comprising external connection nodes (NCEj) connecting the nodes (Nj) to  
 15 one another and handling the transactions between the nodes (Nj), the connection  
 16 agents (NCSi) and the external connection nodes (NCEj) respectively having the same  
 17 basic structure, the same external interface (XI), and adapted to implement the same  
 18 coherency control protocol for the cache memories of the processors, each external  
 19 connection node (NCEj) comprises two identical connection agents (NCSi) connected

20 head-to-tail, one of the two agents (NCS<sub>j</sub>) receiving and filtering transactions sent by  
 21 the node (N<sub>j</sub>) to which it is connected, and the other (NCS<sub>j</sub>) receiving and filtering  
 22 the transactions sent by the other nodes (N<sub>j</sub>) to which it is connected, characterized in  
 23 that it consists of disconnecting one of the first-level multiprocessor modules (Q<sub>Pi</sub>)  
 24 from its connection agent (NCS<sub>i</sub>) to free said connecting agent and of connecting, via  
 25 said freed connection agent, a second given number of processors organized into a  
 26 second given number of multiprocessor modules, also capable of being inserted into  
 27 said interconnection architecture.

1 25. A process for expanding the capacity of a machine comprising a first  
 2 given number of processors on a first level (MI) organized into a first given number  
 3 of multiprocessor modules (Q<sub>Pi</sub>) and capable of being inserted into an interconnection  
 4 architecture comprising a modular interconnection architecture for an expandable  
 5 multiprocessor machine, based on a virtual bus hierarchy, comprising a given number  
 6 of multiprocessor modules (Q<sub>Pi</sub>), each comprising a plurality of processors and  
 7 associated cache memories organized into nodes (N<sub>j</sub>) and distributed on at least two  
 8 interconnection levels: a first interconnection level (MI) corresponding to  
 9 interconnection of the multiprocessor modules (Q<sub>Pi</sub>) within a node (N<sub>j</sub>), and a second  
 10 interconnection level (SI) corresponding to the interconnection of the nodes (N<sub>j</sub>) with  
 11 one another, the first interconnection level (MI) comprising connection agents (NCS<sub>i</sub>)  
 12 connecting the multiprocessor modules (Q<sub>Pi</sub>) to one another and handling the  
 13 transactions between the multiprocessor modules (Q<sub>Pi</sub>), the second interconnection  
 14 level (SI) comprising external connection nodes (NCE<sub>j</sub>) connecting the nodes (N<sub>j</sub>) to  
 15 one another and handling the transactions between the nodes (N<sub>j</sub>), the connection  
 16 agents (NCS<sub>i</sub>) and the external connection nodes (NCE<sub>j</sub>) respectively having the same  
 17 basic structure, the same external interface (XI), and adapted to implement the same  
 18 coherency control protocol for the cache memories of the processors, characterized in  
 19 that it consists of disconnecting one of the first-level multiprocessor modules (Q<sub>Pi</sub>)  
 20 from its connection agent (NCS<sub>i</sub>) to free said connecting agent and of connecting, via  
 21 said freed connection agent, a second given number of processors organized into a  
 22 second given number of multiprocessor modules, also capable of being inserted into  
 23 said interconnection architecture, each connection agent (NCS<sub>i</sub>) comprises an  
 24 associative memory (DD<sub>i</sub>) with a fixed size determined as a function of the number of

25 processors in the multiprocessor module (QPi) to which the connection agent (NCSi)  
 26 is connected, the state of the memories (DDi) being indicative of the presence of the  
 27 last modified data blocks in the cache memories of the multiprocessor module (QPi).

1 26. A process according to claim 24, characterized in the connection agents  
 2 (NCS'j) and (NCS''j) respectively comprise an associative memory (DD'j) and  
 3 (DD''j) with a fixed size determined as a function of the number of processors in the  
 4 multiprocessor module (HBj) to which the connection agents (NCS'j) and (NCS''j)  
 5 are connected, the state of the associated memories (DD'j) and (DD''j) being  
 6 indicative of the presence of the last modified data blocks executed or conversely  
 7 imported.

1 27. A process for expanding the capacity of a machine according to claim 24  
 2 wherein the first and second head-to-tail connection agents (NCS'j and NCS''j) only  
 3 accept transactions for blocks modified in their respective associative memories (DD'j  
 4 and DD''j); modified data blocks in the first connection agent (NCS'j) being exported  
 5 to the requesting multiprocessor module or modules and, conversely, modified data  
 6 blocks in the second connection agent (NCS''j) being imported from the module or  
 7 modules holding the blocks, characterized in that it consists of disconnecting one of  
 8 the first-level multiprocessor modules (QPi) from its connection agent (NCSi) to free  
 9 said connecting agent and of connecting, via this freed connection agent, a second  
 10 given number of processors organized into a second given number of multiprocessor  
 11 modules, also capable of being inserted into said interconnection architecture  
 12 comprising a modular interconnection architecture.

1 28. A process for expanding the capacity of a machine according to claim  
 2 24 wherein the second interconnection level (SI) has a latency that is double the  
 3 latency of the first interconnection level (MI), characterized in that it consists of  
 4 disconnecting one of the first-level multiprocessor modules (QPi) from its connection  
 5 agent (NCSi) to free said connecting agent and of connecting, via this freed  
 6 connection agent, a second given number of processors organized into a second given  
 7 number of multiprocessor modules, also capable of being inserted into said  
 8 interconnection architecture.

1           29.     A process according to claim 23, characterized in that, the second  
2 given number of processors being organized into a second given number of  
3 multiprocessor modules on a second level (SI), it consists of connecting it to the  
4 connection agent (NCS<sub>i</sub>) of the first given number of processors on the first level (MI)  
5 through one of the connection agents (NCS<sub>j</sub>) on the second level.

1           30.     A process according to claim 29, characterized in that, the second  
2 given number of processors also being on the first level (MI), and further comprising  
3 connecting the respective connection agents (NCS<sub>i</sub>) to the first and second given  
4 numbers of processors, the second level (SI) being reduced to a single link.

1           31.     An expandable multi node multiprocessor machine, comprising an  
2 interconnection architecture including a given number of multiprocessor modules  
3 including a modular interconnection architecture for an expandable multiprocessor  
4 machine, based on a virtual bus hierarchy, comprising a given number of  
5 multiprocessor modules (QPi), each module including a plurality of processors and  
6 associated cache memories organized into nodes (Nj) and distributed on at least two  
7 interconnection levels: a first interconnection level (MI) corresponding to  
8 interconnection of the multiprocessor modules (QPi) within a node (Nj), and a second  
9 interconnection level (SI) corresponding to the interconnection of the nodes (Nj) with  
10 one another, the first interconnection level (MI) comprising connection agents (NCS<sub>i</sub>)  
11 connecting the multiprocessor modules (QPi) to one another and handling the  
12 transactions between the multiprocessor modules (QPi), the second interconnection  
13 level (SI) comprising external connection nodes (NCE<sub>j</sub>) connecting the nodes (Nj) to  
14 one another and handling the transactions between the nodes (Nj), the connection  
15 agents (NCS<sub>i</sub>) and the external connection nodes (NCE<sub>j</sub>) respectively having the same  
16 basic structure, the same external interface (XI), and adapted to implement the same  
17 coherency control protocol for the cache memories of the processors.

1           32.     An expandable multinode multiprocessor machine as set forth in claim  
2 31, characterized in that each external connection node (NCE<sub>j</sub>) comprises two  
3 identical connection agents (NCS<sub>i</sub>) connected head-to-tail, one of the two agents  
4 (NCS<sub>j</sub>) receiving and filtering transactions sent by the node (Nj) to which it is

5 connected, and the other agent (NCS"j) receiving and filtering the transactions sent by  
6 the other nodes (Nj) to which it is connected.

1 33. An expandable multinode multiprocessor machine as set forth in claim  
2 31, characterized in that each connection agent (NCSi) comprises an associative  
3 memory (DDi) with a fixed size determined as a function of the number of processors  
4 in the multiprocessor module (QPi) to which the connection agent (NCSi) is  
5 connected, the state of the memories (DDi) being indicative of the presence of the last  
6 modified data blocks in the cache memories of the multiprocessor module (QPi).

1 34. An expandable multinode multiprocessor machine as set forth in claim  
2 31, characterized in that each connection agent (NCSi) comprises an associative  
3 memory (DDi) with a fixed size determined as a function of the number of processors  
4 in the multiprocessor module (QPi) to which the connection agent (NCSi) is  
5 connected, the state of the memories (DDi) being indicative of the presence of the last  
6 modified data blocks in the cache memories of the multiprocessor module (QPi).

1 35. An expandable multinode multiprocessor machine as set forth in claim  
2 31, characterized in that the first and second head-to-tail connection agents (NCS'j  
3 and NCS"j) only accept transactions for blocks modified in their respective  
4 associative memories (DD'j and DD"j); modified data blocks in the first connection  
5 agent (NCS'j) being exported to the requesting multiprocessor module or modules  
6 and, conversely, modified data blocks in the second connection agent (NCS"j) being  
7 imported from the module or modules holding the blocks.

1 36. An expandable multinode multiprocessor machine as set forth in claim  
2 31, characterized in that the second interconnection level (SI) has a latency that is  
3 double the latency of the first interconnection level (MI).

1 37 A process for tracing data blocks in an interconnection architecture for  
2 an expandable microprocessor machine, based on a virtual bus hierarchy, comprising  
3 a given number of multiprocessor modules (QPi), each module including a plurality  
4 of processors and associated cache memories organized into nodes (Nj) and

5 distributed on at least two interconnection levels: a first interconnection level (MI)  
 6 corresponding to interconnection of the multiprocessor modules (QPi) within a node  
 7 (Nj), and a second interconnection level (SI) corresponding to the interconnection of  
 8 the nodes (Nj) with one another, the first interconnection level (MI) comprising  
 9 connection agents (NCSi) connecting the multiprocessor modules (QPi) to one  
 10 another and handling the transactions between the multiprocessor modules (QPi), the  
 11 second interconnection level (SI) comprising external connection nodes (NCEj)  
 12 connecting the nodes (Nj) to one another and handling the transactions between the  
 13 nodes (Nj), the connection agents (NCSi) and the external connection nodes (NCEj)  
 14 respectively having the same basic structure, the same external interface (XI), and  
 15 adapted to implement the same coherency control protocol for the cache memories of  
 16 the processors, comprising duplicating on the first level in the associative memories  
 17 (DDi) only modified data blocks in the cache memories of the multiprocessor  
 18 modules (QPi) and tracing only the modified blocks inside the node (Nj).

1 38. A process for tracing data blocks as set forth in claim 37 wherein each  
 2 external connection node (NCEj) comprises two identical connection agents (NCSi)  
 3 connected head-to-tail, one of the two agents (NCS'j) receiving and filtering  
 4 transactions sent by the node (Nj) to which it is connected, and the other agent  
 5 (NCS''j) receiving and filtering the transactions sent by the other nodes (Nj) to which  
 6 it is connected.

1 39. A process for tracing data blocks as set forth in claim 37 wherein each  
 2 connection agent (NCSi) comprises an associative memory (DDi) with a fixed size  
 3 determined as a function of the number of processors in the multiprocessor module  
 4 (QPi) to which the connection agent (NCSi) is connected, the state of the memories  
 5 (DDi) being indicative of the presence of the last modified data blocks in the cache  
 6 memories of the multiprocessor module (QPi).

1 40. A process for tracing data blocks as set forth in claim 38, characterized  
 2 in that the first and second head-to-tail connection agents (NCS'j and NCS''j) only  
 3 accept transactions for blocks modified in their respective associative memories (DD'j  
 4 and DD''j); modified data blocks in the first connection agent (NCS'j) being exported



5 to the requesting multiprocessor module or modules and, conversely, modified data  
 6 blocks in the second connection agent (NCS"j) being imported from the module or  
 7 modules holding the blocks

1 41. A process for tracing data blocks as set forth in claim 38, characterized  
 2 in that the first and second head-to-tail connection agents (NCS'j and NCS"j) only  
 3 accept transactions for blocks modified in their respective associative memories (DD'j  
 4 and DD"j); modified data blocks in the first connection agent (NCS'j) being exported  
 5 to the requesting multiprocessor module or modules and, conversely, modified data  
 6 blocks in the second connection agent (NCS"j) being imported from the module or  
 7 modules holding the blocks.

1 42. A process for tracing data blocks as set forth in claim 13, characterized  
 2 in that the second interconnection level (SI) has a latency that is double the latency of  
 3 the first interconnection level (MI).

1 43. A process for tracing data blocks in a modular interconnection  
 2 architecture for an expandable multiprocessor machine, based on a virtual bus  
 3 hierarchy, comprising a given number of multiprocessor modules (QPi), each module  
 4 including a plurality of processors and associated cache memories organized into  
 5 nodes (Nj) and distributed on at least two interconnection levels: a first  
 6 interconnection level (MI) corresponding to interconnection of the multiprocessor  
 7 modules (QPi) within a node (Nj), and a second interconnection level (SI)  
 8 corresponding to the interconnection of the nodes (Nj) with one another, the first  
 9 interconnection level (MI) comprising connection agents (NCSi) connecting the  
 10 multiprocessor modules (QPi) to one another and handling the transactions between  
 11 the multiprocessor modules (QPi), the second interconnection level (SI) comprising  
 12 external connection nodes (NCEj) connecting the nodes (Nj) to one another and  
 13 handling the transactions between the nodes (Nj), the connection agents (NCSi) and  
 14 the external connection nodes (NCEj) respectively having the same basic structure,  
 15 the same external interface (XI), and adapted to implement the same coherency  
 16 control protocol for the cache memories of the processors, characterized in that it  
 17 consists, on the second level (SI), of duplicating in the associative memories (DD'j

18 and DD"J) of the connection agents (NCS' and NCS"j) of each external connection  
 19 node (NCEj) only the modified blocks exported, or conversely imported, and of  
 20 tracing only the modified blocks exported, or conversely imported, between each  
 21 node (Nj) of the machine.

1 44. A process for tracing data blocks as set forth in claim 43, wherein each  
 2 external connection node (NCEj) comprises two identical connection agents (NCSi)  
 3 connected head-to-tail, one of the two agents (NCS'j) receiving and filtering  
 4 transactions sent by the node (Nj) to which it is connected, and the other agent  
 5 (NCS"j) receiving and filtering the transactions sent by the other nodes (Nj) to which  
 6 it is connected.

1 45. A process for tracing data blocks as set forth in claim 43, wherein each  
 2 connection agent (NCSi) comprises an associative memory (DDi) with a fixed size  
 3 determined as a function of the number of processors in the multiprocessor module  
 4 (QPi) to which the connection agent (NCSi) is connected, the state of the memories  
 5 (DDi) being indicative of the presence of the last modified data blocks in the cache  
 6 memories of the multiprocessor module (QPi).

1 46. A process for tracing data blocks as set forth in claim 44, wherein each  
 2 connection agent (NCSi) comprises an associative memory (DDi) with a fixed size  
 3 determined as a function of the number of processors in the multiprocessor module  
 4 (QPi) to which the connection agent (NCSi) is connected, the state of the memories  
 5 (DDi) being indicative of the presence of the last modified data blocks in the cache  
 6 memories of the multiprocessor module (QPi).

1 47. A process for tracing data blocks as set forth in claim 44, wherein the  
 2 first and second head-to-tail connection agents (NCS'j and NCS"j) only accept  
 3 transactions for blocks modified in their respective associative memories (DD'j and  
 4 DD"j); modified data blocks in the first connection agent (NCS'j) being exported to  
 5 the requesting multiprocessor module or modules and, conversely, modified data  
 6 blocks in the second connection agent (NCS"j) being imported from the module or  
 7 modules holding the blocks.

- A3  
emld.
- 1 48. A process for tracing data blocks as set forth in claim 43, wherein the
  - 2 second interconnection level (SI) has a latency that is double the latency of the first
  - 3 interconnection level (MI).--
- 

00940 265900